In the specification:

IDC-A1,AMD Amend the paragraph on page 1, lines 10 to 21 as follows:

As transistor device densities continue to increase, minor fabrication and operational defects can ~~have~~ impact transistor operation inversely proportional to ~~with~~ the size of the transistor. One of the well-known problems for small field effect transistors is channel hot carrier effects. For example, when a conventional metal oxide semiconductor field effect transistor (MOSFET) structure is scaled down to one micron or less, the potential energy of an electron changes dramatically when it hits the n^+ drain boundaries. This sudden change in potential energy in a short distance tends to create a high electric field. This causes the electrons to behave differently within the semiconductor lattice. Electrons which have been activated by high electric fields are referred to as "hot electrons", and can, for example, penetrate into or through the gate dielectric. Electrons that penetrate into, but not through, the gate dielectric can cause the gate dielectrics to store charge over time, until the transistor ultimately fails.

NRB
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IDC-A2,AMD Amend the paragraph on page 4, lines ~~11~~ 9 to ~~19~~ 18 as follows:

FIG. 1 depicts a schematic cross-sectional view of a transistor 10 in accordance with an aspect of the present invention. The transistor 10 can be a p-channel transistor or an n-channel transistor. For purposes of simplicity of explanation, the following discussion of FIG. 1 will assume an n-channel transistor, such as an NMOS. The transistor 10 includes a gate structure 12 that is disposed over a gate dielectric layer 14. To form the gate structure 12, a corresponding area is patterned and then later doped. The gate structure 12 can include a poly silicon gate (*e.g.*, polygate). The poly gate is doped to render it conductive, such as through diffusion or ~~of~~ ion implantation. The particular doping of the polygate may depend on the type of device (*e.g.*, whether it is an n-channel or p-channel device